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Multilevel Inverters with Imbricated Switching Cells, PWM and DPWM-Controlled

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Introduction

Multilevel voltage inverters with imbricated switching cells are destined to high and very high-power applications. These structures led to the normalization of the voltage distribution when the semiconductor devices are blocked and to the improvement of the total factor of harmonic distortions as compared to the classic inverter structures. Static power converters for high voltages generally need on-off switches (semiconductor devices) that can function under these voltages. If these switches are not available, different converter topologies must be developed, where only a voltage fraction is applied to each switch [1].

Switches connected in series

One of the possible solutions is connecting in series several synchronously-controlled switches [2], in order to obtain a high voltage switch. They must start commutation at the same time, otherwise there may be voltage balance problems, control problems and du/dt stress, generated for each commutation. Fig. 1 presents two circuits illustrating how switches can be connected in series.
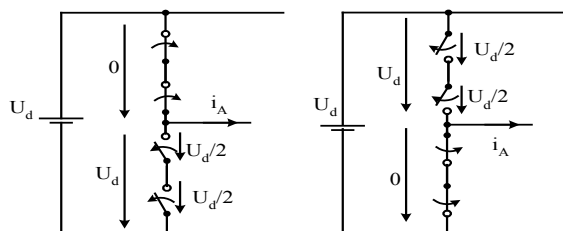

Fig. 1. Switches connected in series

It is difficult to realize the static or dynamic balance of voltages on the switches, as it requires special techniques.
- Static balancing can be accomplished by connecting high-value resistances in parallel with every switch;
- Dynamic balancing raises more serious problems.

All switches must commute at the same time. If this condition is not fulfilled, the first switch that becomes blocked (or the one that commutes last) will bear the entire voltage.

In most of the cases, commutations cannot be synchronized by the mere synchronization of control signals. Semiconductor devices must be selected as pairs having the same conduction/blocking time, otherwise we must use special control circuits, capable of compensating the differences between these times [3].

Multilevel voltage inverters with imbricated switching cells

In order to obtain a better distribution of voltage on each switch, new converter structures were developed. The basic structure of a three-level bridge arm is presented in Fig. 2 and is made up of two imbricated switching cells: (A_1, B_1) and (A_2, B_2). Within each switching cell there are two complementary switches, bidirectional in current and unidirectional in voltage (transistor + diode, connected in antiparallel)[4].

Consequently, this topology solves the problem specific to structures connected in series, namely the static and dynamic balancing of voltages when switches are blocked.
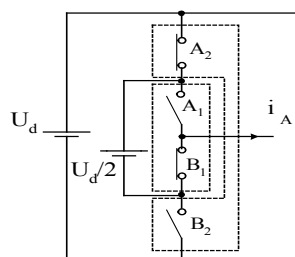

Fig. 2. Structure of a three-phase voltage inverter, with imbricated switching cells - 3 levels

The switches that make up different switching cells can be controlled at different points in time. If the voltage applied on a switch is $U_d/2$ (and assuming the conduction

voltage is zero), the voltage supplied by the switching cell (B_1, B_2) can be 0, $U_d/2$ or U_d according to the number of switches turned off (0, 1 or 2), which is similar to the classic case of the three-level inverter. In practice, the voltage supply $U_d/2$ must be replaced by a capacitor C charged at $U_d/2$.

In order to determine the voltage steps that can be obtained in the general case, we considered in Fig. 3 that voltages on the capacitors fulfill the following condition:

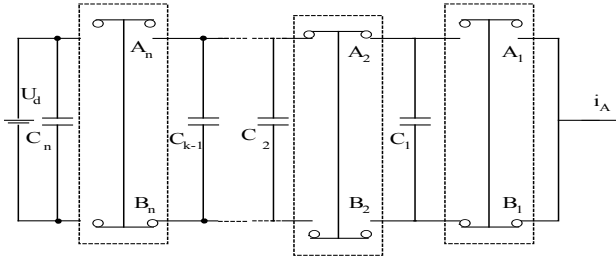$$U_{Ck} = k\frac{U_d}{n}, k = 1,...n \qquad (1)$$

Fig. 3. Structure of an inverter arm containing *n* imbricated cells (n+1 voltage levels)

The voltage applied to the blocked switch within the switching cell k depends only on the voltage on the capacitor C_k and C_{k-1}, and is calculated as

$$U_{OFFk} = k\frac{U_d}{n} - (k-1)\frac{U_d}{n} = \frac{U_d}{n}. \qquad (2)$$

Knowing that the voltage on a blocked switch is U_d/n (and assuming that voltage on the switch in conduction state is zero), one can easily understand how the converter works: the voltage released by a multilevel switching cell $(B_1, B_2,..., B_n)$, whatever the point in time, is calculated by multiplying the voltage step U_d/n by the number of switches blocked. This shows that there are n+1 possible voltage levels: 0, U_d/n, $2U_d/n$,..., U_d.

Control strategy for the multilevel inverter

The control of multilevel switching cells must fulfill simultaneously two important requirements:
− compatibility with voltage $U_{Ck}=kU_d/n=const.$, k=1,...n;
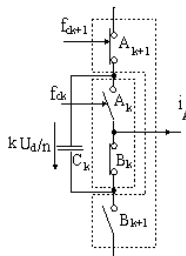− optimization of the harmonic spectrum.

Fig. 4. Connecting capacitor C_k

Each capacitor C_k is connected between the pairs of switches k and k+1, Fig. 4.

According to their state, the current through the capacitor can be: $-I_A$, 0 or $+I_A$ (we assumed $I_A=i_A$ =const.

for the duration of a switching period T_p). Thus, the current through the capacitor can be expressed as:

$$i_{Ck} = (f_{Ck} - f_{Ck+1})I_A, \qquad (3)$$

where f_{Ck} and f_{Ck+1} stand for the connection functions for A_k and A_{k+1} switches and can only have two values: 0 or 1 (according to the state of the switches) [5]. For instance, if $f_{Ck} =1$ when the A_k switch is off and $f_{Ck}=0$ when the A_k switch is on.

For multilevel converters, in order to obtain equal conduction durations for all the cells of an arm, it is necessary to use *"n"* carrier waves dephased by T_p/n and, thus, stability for capacitors $C_1, ...,C_n$ is attained.

The power circuit of the three-level inverter with imbricated cells and the control strategy are presented in Fig. 5.
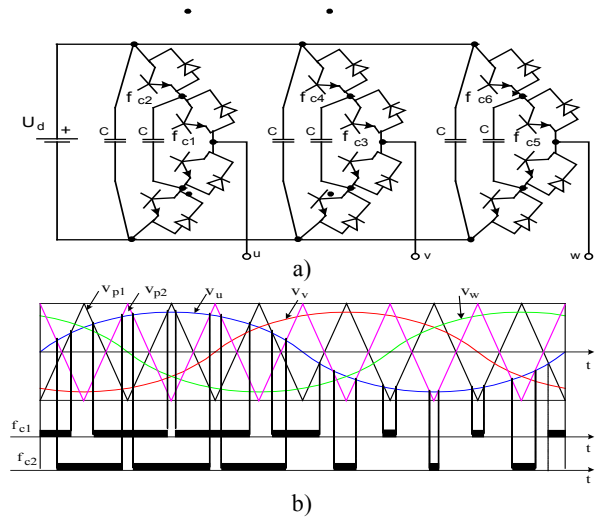

Fig. 5. Three-phase voltage inverter with three-level imbricated switching cells and control strategy

The PWM control strategy adopted for an arm consists in comparing a reference (sinusoidal) wave to two carrier (triangular symmetric) waves dephased by 180° [6]. These comparisons lead to two connection functions for arm f_{c1} and f_{c2} defined as follows:

$$\begin{cases} v_u > v_{p1}, \text{ therefore } f_{c1} = 1; \; v_u > v_{p2}, \text{ therefore } f_{c2} =1, \\ \\ v_u < v_{p1}, \text{ therefore } f_{c1} = 0; \; v_u < v_{p2}, \text{ therefore } f_{c2} = 0. \end{cases} \qquad (4)$$

The performances of the system presented can be improved (reduced harmonic level, increased efficiency, etc.) if, as part of the command strategy, the sinusoidal reference wave is replaced by a modified sinusoidal wave (discontinuous command techniques DPWM) [7], described in (5)

$$s_1 = \begin{cases} 1, & 0 \le \omega_m t \le \pi/6, \\ \sqrt{3}m_a\cos\omega_m t + m_a\sin\omega_m t - 1, & \pi/6 \le \omega_m t \le \pi/2, \\ \sqrt{3}m_a\cos\omega_m t - m_a\sin\omega_m t + 1, & \pi/2 \le \omega_m t \le 5\pi/6, \\ 1, & 5\pi/6 \le \omega_m t \le 7\pi/6, \\ \sqrt{3}m_a\cos\omega_m t - m_a\sin\omega_m t + 1, & 7\pi/6 \le \omega_m t \le 3\pi/2, \\ \sqrt{3}m_a\cos\omega_m t + m_a\sin\omega_m t - 1, & 3\pi/2 \le \omega_m t \le 11\pi/6, \\ 1, & 11\pi/6 \le \omega_m t \le 2\pi. \end{cases} \qquad (5)$$

Fig. 8 presents the control strategy applied to the inverter illustrated in Fig. 5, using the modified sinusoidal wave s1 and its corresponding waveform v_{us1}, v_{vs1}, v_{ws1}, for the given situation [8].
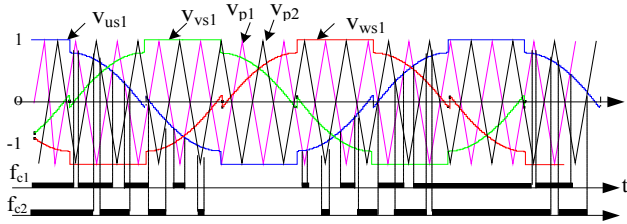

Fig. 6. Control strategy of the three-phase voltage inverter with three-level imbricated switching cells, using signal s1

Simulation results

Starting from the study presented and using the simulation environment Pspice, we shall present a compared analysis of the functioning of the two-level three-phase inverter [9]. For the simulation of the inverter in Fig. 5, we used the sinusoidal PWM and DPWM control strategies and we took into account the following values: inductive load R=10Ω, L=10mH, amplitude modulation index m_a=0.95, carrier wave frequency 50Hz, switching frequency 5kHz, and supply voltage amplitude U_d= 310V.

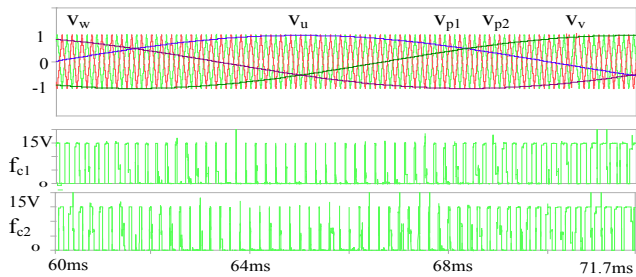Fig. 7 presents the waveforms of the carrier signals v_{p1}, v_{p2},

Fig. 7. Waveforms of carrier, modulating and command signals using PWM sinusoidal control

of the sinusoidal modulating signals on 50Hz, v_u, v_v, v_w, and of the control signals on switches A_1, A_2, implemented by the transistors of the inverter presented in Fig. 5, using the sinusoidal PWM control strategy.
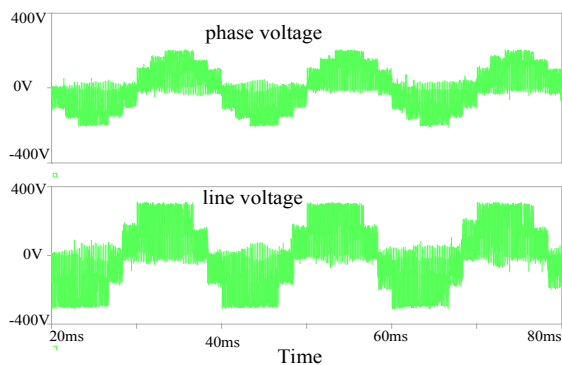

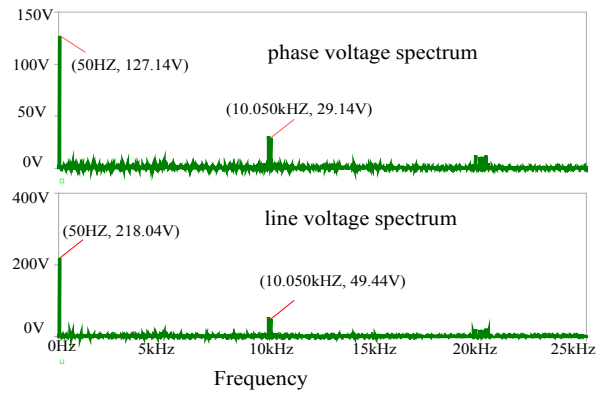**Fig. 8.** Waveforms of phase and line voltage using PWM sinusoidal control

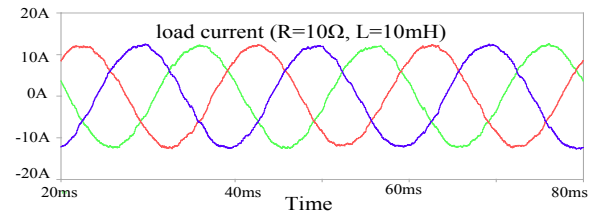**Fig. 9.** Phase and line voltage spectrum using PWM sinusoidal control

Fig. 10. Load current using the PWM sinusoidal control

Figures 8, 9 and 10 present the main waveforms obtained by simulating the functioning of the inverter in Fig. 5, using the sinusoidal PWM control strategy.

Fig. 11 presents the waveforms of the carrier signals v_{p1}, v_{p2}, of the modified sinusoidal modulating signals on 50Hz, v_{us1}, v_{vs1}, v_{ws1}, and the control signals on switches A_1, A_2, implemented by the transistors of the inverter presented in Fig. 5, using the DPWM control strategy.
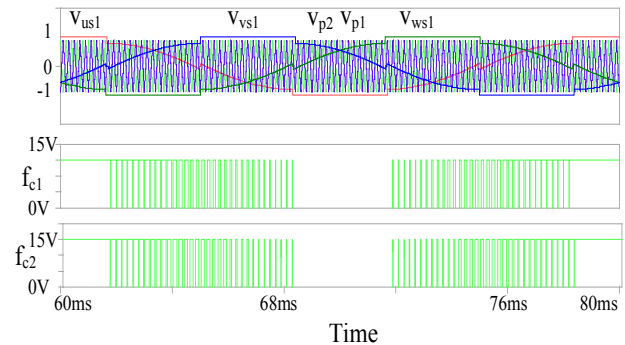

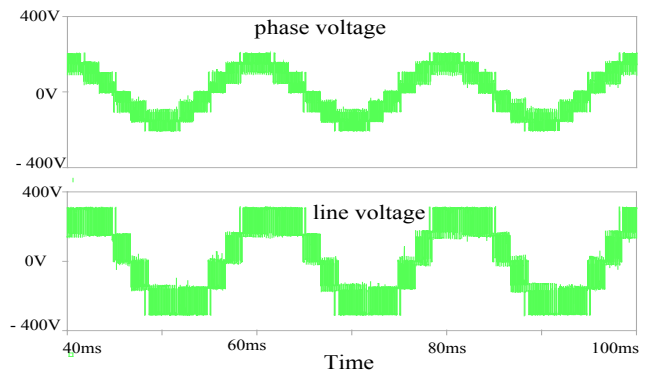**Fig. 11.** Waveforms of the carrier, modulating and control signals using DPWM control

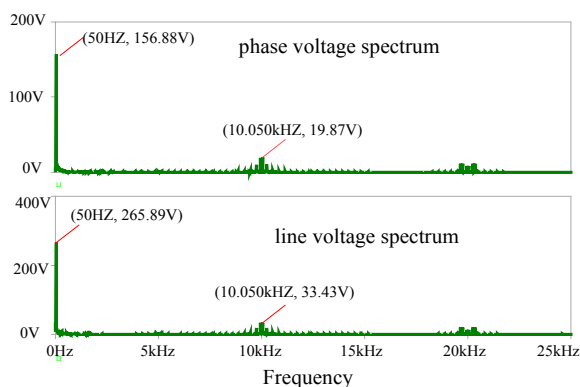**Fig. 12.** Waveforms of the phase and line voltage using DPWM control

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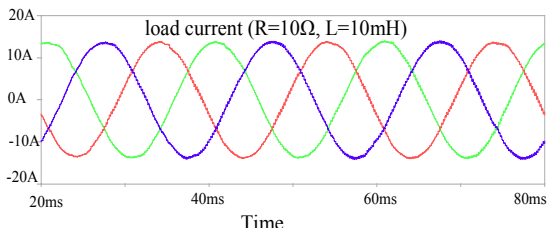**Fig. 13.** Phase and line voltage spectrum using DPWM control

Fig. 14. Load current using DPWM control

Figures 12, 13 and 14 present the main waveforms obtained by simulating the functioning of the inverter in Fig. 5, using the DPWM control strategy.

Conclusions

The results of the simulation show that, even though each switch (transistor) is controlled with a switching frequency of 5kHz, the harmonic spectrum of the phase and line voltages does not include harmonics due to the switching around this harmonic. Therefore, we can state that the three-level inverter structure with imbricated switching cells doubles the output switching frequency.
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This determines fewer current/torque variations, diminished losses in the motor/converter and allows the use of devices of high voltage, but low switching frequencies. On the one hand, the DPWM control strategy allows the increase of the voltage fundamental due to the reduction of the harmonic amplitude at a double switching frequency and, on the other hand, the waveform of the output voltage approximates the sinusoidal waveform more accurately.

References

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O. Ursaru, C. Aghion. Multilevel Inverters with Imbricated Switching Cells, PWM and DPWM-Controlled // Electronics and Electrical Engineering. – Kaunas: Technologija, 2010. – No. 8(104). – P. 23–26.
This paper analyzes the functioning of multilevel voltage inverters with imbricated switching cells, destined for high and very high-power applications. Based on the theoretic principles, it presents the functioning of the three-phase voltage inverter with three-level imbricated cells. The simulations based on the sinusoidal PWM and DPWM control strategies yielded results that showed the main advantages of this type of inverters.. Ill. 14, bibl. 9 (in English; abstracts in English, Russian and Lithuanian).

О. Урсару, Ц. Агхион. Многоуровневые инверторы на основе PWM и управляемы DPWM // Электроника и электротехника. – Каунас: Технология, 2010. – № 8(104). – С. 23–26.
Анализируется функционирование многоуровневых инверторов напряжения с вложенными ячейками переключения, предназначенных для высокого напряжения и очень мощных сигналов. На основании теоретических основ, разработаны основы функционирования 3-фазного напряжения инвертора с трехуровневыми ячейками переключения. Моделированием на основе синусоидального ШИМ и стратегии управления DPWM получены результаты, которые показали основные преимущества инверторов этого вида. Ил. 14, библ. 9 (на английском языке; рефераты на английском, русском и литовском яз.).

O. Ursaru, C. Aghion. PWM ir DPWM valdomi daugelio lygmenų inverteriai // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2010. – Nr. 8(104). – P. 23–26.
Analizuojami daugelio lygmenų įtampos inverteriai, skirti aukštos įtampos ir didelės galios signalų komutacijai. Teoriškai įrodyta, kad trijų fazių įtampos inverterį bei trijų lygių perjungimo grandines tikslinga projektuoti, naudojant PWM ir DPWM valdymo strategiją. Il. 14, bibl. 9 (anglų kalba; santraukos anglų, rusų ir lietuvių k.).