Study of digital technology implementation of peak current control method applied to synchronous buck converter

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***Abstract*-Lately, digital control technology has advanced greatly in the field of power electronics[14], enabling implementation of more and more common method to control electronic converters.This paper presents the modeling and the simulation of peak current control method applied to a synchronous buck converter with digital control, and its practical implementation. For simulation, the C language source code was designed for the perturbations compensating function, the duty cycle calculation applied to PWM generator, and variable current reference.**

I. INTRODUCTION

Modeling and simulation of peak current method applied to synchronous buck converter [11]-[13] was developed in Matlab Simulink R2010a program, and the practical implementation by using a DSP from Microchip dsPIC33FJ16GS502[1]-[4]. The block diagram of principle from which we started implementing the control method is shown in Fig. 1 [5], [6]. The switching frequency of MOSFET transistors was chosen 50kHz . The DC voltage applied to the converter at the input was 28V and output was dimensioned so that the output would be a stabilized voltage of 12V. To stress the converter up to 288W, the load rezistor chosed was 0.5Ω. To analyze performance of control method, we will vary quickly the load resistor from 100Ω to 0.5Ω and vice versa, thus obtaining a variable power output from 1.44W to 288W, and vice versa.

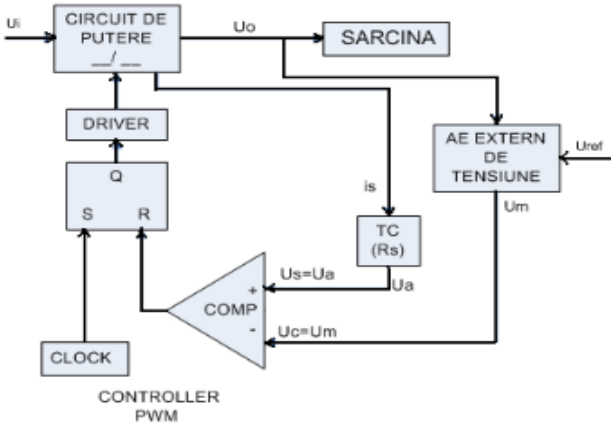

Fig. 1: The block diagram of peak current control

II. Modeling converter command:

The simulated scheme of control method applied to the buck converter is shown in Fig.2 [8]-[10]. All the built blocks in Matlab Simulink were chosen based on existing functional blocks in DSP to simulate with more accurately the real case, and perturbations compensation logic from output and calculated duty cycle applied to the PWM generator were implemented using a software function coded in C language.

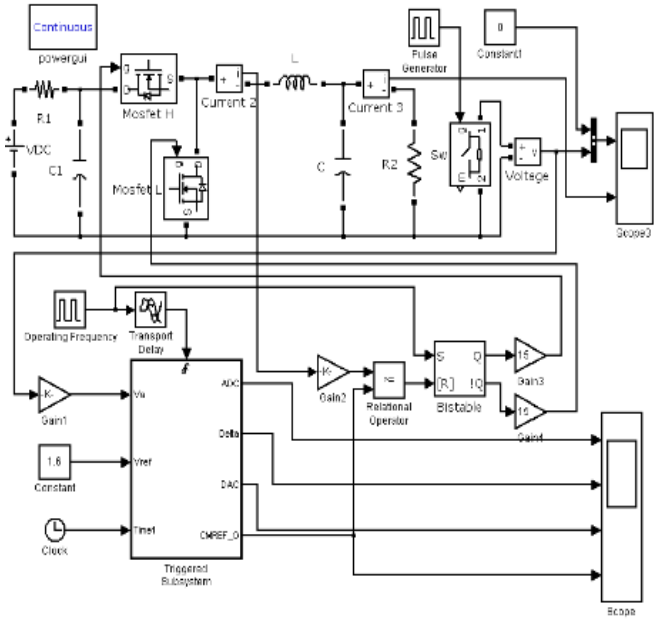

Fig. 2: Simulation scheme

The "High Speed PWM"[4] bloc working in a complementary way was modeled using the "Bistable" block. The "High Speed Comparator"[4] block was implemented using the "Relational Operator" block that makes the comparison between the signal from the block "Gain2", which represents the inductor current divided suitable, and the variable current reference signal from the "CMREF_O", which shapes the DAC block within the DSP[4]. Modeling the function that performs the logic for

compensating the output perturbations, calculation of duty cycle applied to the PWM generator, the variable current reference and DAC block have been implemented using "Triggered Bubsystem" block, inside which there is "MATLAB Embedded Function" block, represented in Fig. 3, in which the function is written in C language. The ADC circuit inside the DSP[4] was modeled with the "Sample & Hold" block (Fig. 3), and using "Transport Delay" block (Fig. 2) were modeled triggering sampling time of ADC, against of rissing edge time of MOSFET switch from high side, plus specific converting time delay of ADC[4], which in this example is 1us from switching time plus 1us of time during the conversion. The triggering frequency of the "Triggered Bubsystem" block is equal to the transistor switching frequency. The quick variation of load resistance from 0.5Ω to 100Ω and vice versa, was achieved by connecting in parallel with the load resistance a switch with 0.5Ω contact resistance, its switching being achieved through pulse generator.

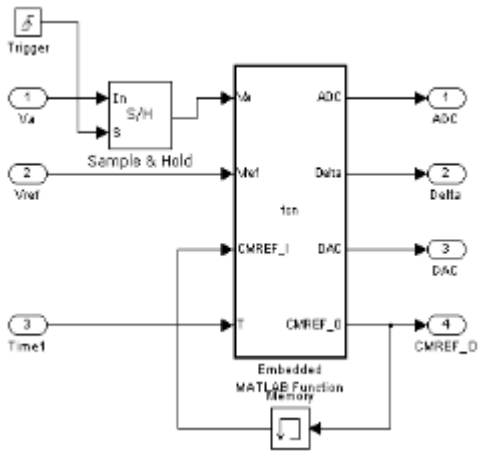

Fig. 3: Content of "Triggered Bubsystem" block

The source code written in C language, contained in "Embadded Fuction MATLAB" block is presented below:

```
% Outputs                    Inputs
function [ADC, Delta DAC CMREF_O] = FCN (Va, Vref, CMREF_I, T)

  Temp_Vref = Vref;
  Temp_ADC = VA;
  Temp_CMREF_I = CMREF_I;
  Gain = 18;
  Current_limit_M = 48;

  if (T <= 0.01)
    Temp_Vref = 0.8;
  end

  if (Temp_ADC <= Vref)
    Temp_Delta = (Vref - Temp_ADC) * Gain;
    Temp_CMREF_O = Temp_CMREF_I + Temp_Delta;
  else
    Temp_Delta = (Temp_ADC - Vref) * Gain;
    if (Temp_CMREF_I> = Temp_Delta)
        Temp_CMREF_O = Temp_CMREF_I - Temp_Delta;
    else
      Temp_CMREF_O = 0;
    end
  end

  if (Temp_CMREF_O> Current_limit_M)
    Temp_CMREF_O = Current_limit_M;
  end

  CMREF_O = Temp_CMREF_O;
  Delta = Temp_Delta;
  ADC = VA;
  DAC = CMREF_I;
end
```

III. Simulation results:

At a load variation from 0W to 288W, and vice versa, the waveforms for the voltage and current of the load resistance are represented in Fig.4. Note that at a quick variation of load from 0 to 100%, equivalent to a current variation from 0A to 24A, the output voltage ripple amplitude is 1V, followed by some oscillations, compensated in about 3ms. The load variation from 100% to 0%, equivalent to a current variation from 24A to 0A, has a positive ripple voltage of 1V, which is amortized linearly in about 1.2ms. These ripples are found proportionally in a load current.

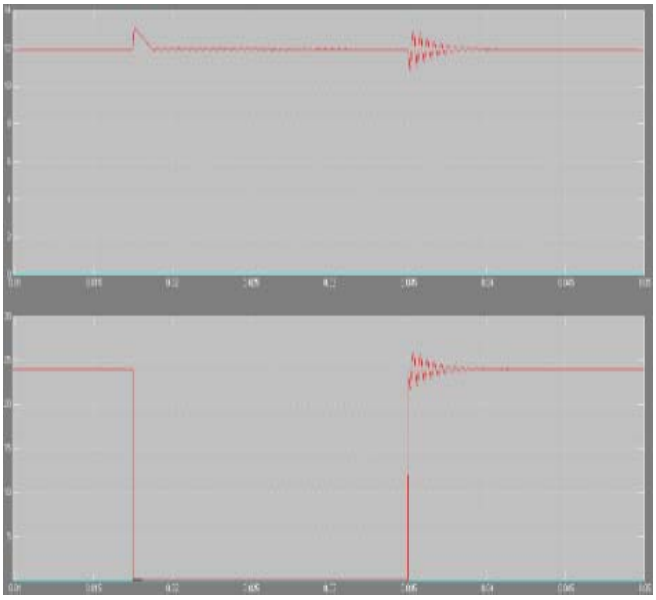

Fig. 4 : Wave forms for the voltage and current of the load resistance plotted in Matlab

IV. Practical realization:

The practical scheme achieved is presented in Fig.5. We observe the MOSFET transistors IRF3205 with snubber circuits associated, controlled by drivers with optical isolation HCPL3120, for good command of entrance in conduction and blocking the conduction of the transistors. The current sensor is LA 25-NP, connected in series with the inductor of converter, to collect a signal as clean as possible in terms of noise. For the electronic relay that switch the load resistance of 0.5Ω is used a MOSFET transistor IRF3205 with snubber circuit associated, commanded through TC4427 driver. The function that performs the logic compensation of output perturbation, applied to calculate the duty cycle for PWM generator, and variable current reference and DAC block, is called in ADC interrupt routine block, with a delay of 2us from the rissing edge moment of the High Side transistor conduction, delay used for sampling signals as clean after switching specific

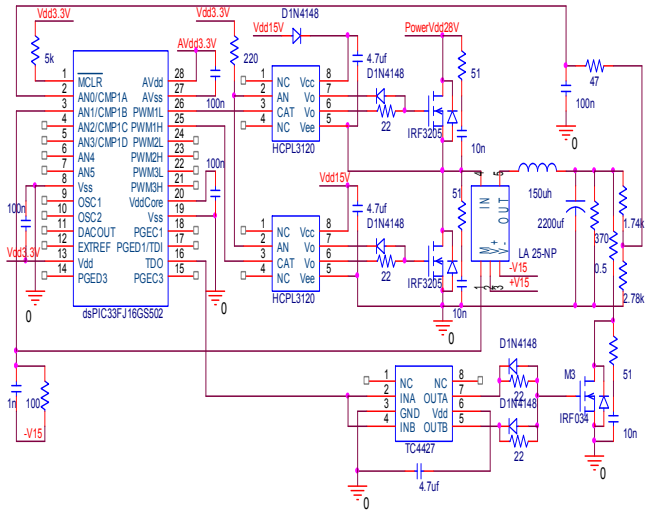

Fig. 5: The practical scheme

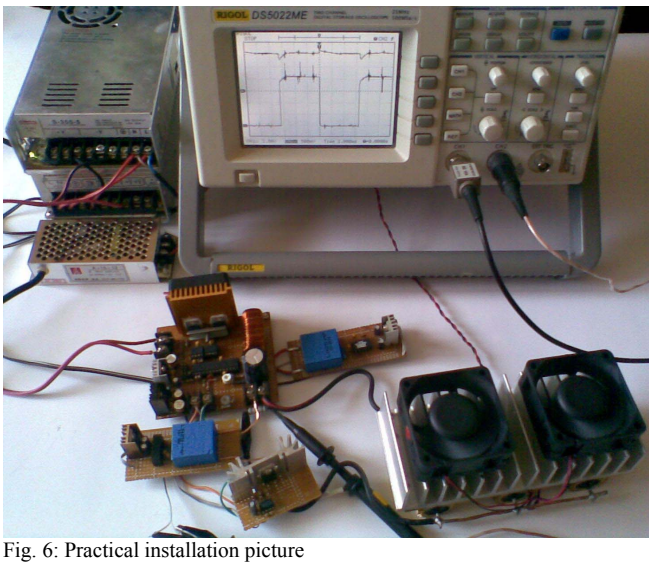

Fig. 6: Practical installation picture

oscillations disappear.The frequency of interrupt routine is equal to converter switching frequency 50kHz. The source code written in C of this routine is identical to the one written in Matlab Simulink and therefore was not presented. Picture of practical installation is shown in Fig. 6. The flowchart of the control software algoritm is presented in Fig. 7 a) and Fig. 7 b).

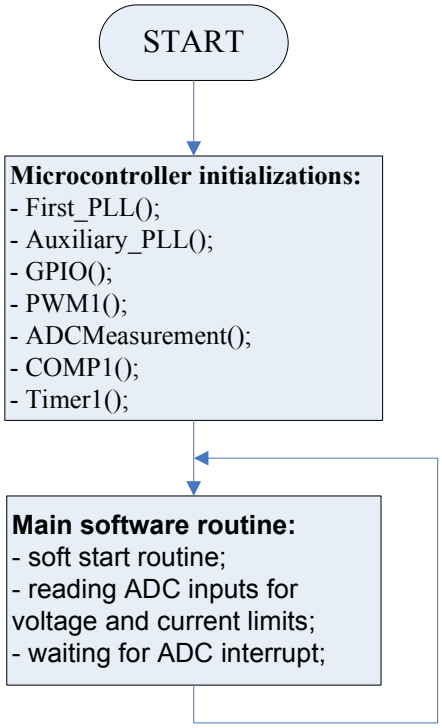

Fig. 7 a): Software control

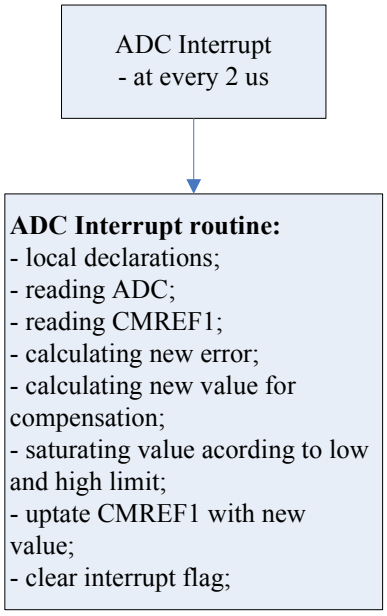

Fig. 7 b): Flowchart of ADC Interrupt

V. Practical results:

In practice, even if the same load resistance of 0.5Ω was used, due to contact resistance and cables, was obtain a variance from 0A to 21A, and reverse, the equivalent variation of power from 0W to 252W and vice versa. The electronic switch was built using a power MOSFET transistor to eliminate the switch oscillations, specific for mechanical switches, and to ensure more vertical fronts at times switching. Waveforms of voltage and current from load resistance are presented in Fig. 8. Note that at a load variation from 0 to 100%, the negative ripple amplitude of the output voltage is 0.9V , compensated in about 1ms. At a load variation from 100% to 0% there is a positive ripple of 0.4V voltage, compensated linearly in about 2ms. These ripples are found proportionally in load current.

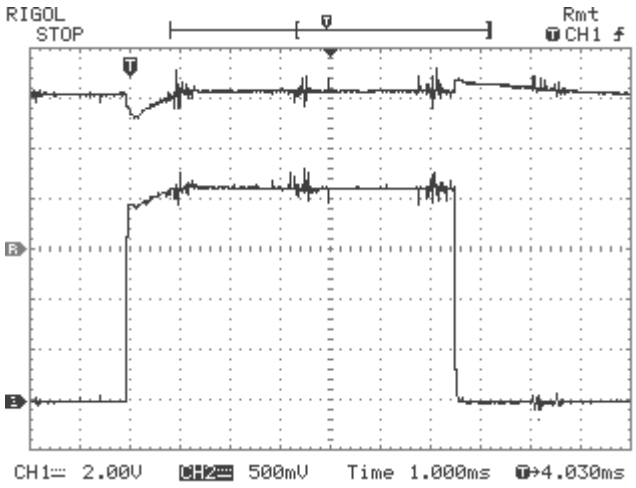

Fig. 8: The waveforms for the voltage and current of the load resistance obtained practically

V. Conclusions:

Implementation in digital technique of power voltage converters controllers at medium and high power has many advantages in terms of such a command performance, precise, with a high immunity to electromagnetic interference because all functional blocks are integrated into the same chip. Digital controllers still show the advantages of ease and flexibility of implementation and scalability. This implementation way allows carrying out high performance algorithms for power management and an increased possibility of interfacing the controlled converters with power supplied systems and communication with the external environment.

ACKNOWLEDGMENT

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VI. References:

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