Fast Interrupts #1
CAPCOM Interference

Fast Interrupts and CAPCOM Interference

When using the fast interrupt input options on port 2, there is no automatic disabling of the associated capture/compare functions related to these pins. Instead, the interrupt requests from the fast interrupt input and the associated capture/compare channel are ORed. This means, if one of the fast interrupt inputs is selected via the EXICON register and additionally the capture/compare register associated with this pin is programmed for a capture or compare function via the respective CCMODx bit field in the CCMx register, unexpected interrupt requests could occur due to a capture or compare event.

Therefore, it is recommended to always disable any capture or compare function associated to a pin when using this pin as a fast interrupt input.

If someone wants to use this double function on purpose, please note the following remarks:

- there is no distinction given between a fast interrupt input request and a capture/compare request
- the capture function requires to hold a level at the input pin for a minimum duration of one CAPCOM cycle (400 ns @ 20 MHz CPU Clock) in order to safely recognize a transition. For the fast interrupt input, a minimum hold time of two TCL is sufficient, but in order to also force a capture function on a transition of the pin, the hold time for the capture input must be obeyed.
- when programming the fast interrupt input and the capture function to be active at the same transition, it is unpredictible whether one or two interrupt requests will be generated. The reason for this are the different sampling rates for the fast interrupt input and capture input. If the transition occurs such that it is recognized immediately by both, the fast interrupt input and the capture input, one will see only one interrupt request. If the fast interrupt input is recognized immediately, but the capture input sample is just missed and then recognized one CAPCOM cycle later, the interrupt request could be set twice. Thus, if the first interrupt request is acknowledged by the CPU very fast, then it will be reset by hardware, but set again due to the capture interrupt request.