SIEMENS

Microcontrollers

ApNote AP1605

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APXXXX01.EXE available

Instruction Set - ATOMIC / EXTEND - BTRAP

During ATOMIC or EXTEND sequences, no interrupts, PEC transfers, or class A traps will be acknowledged by the CPU.

C.Meinold / Siemens HL MCB AT

ATOMIC/EXTEND Instructions in BTRAP Service Routine

As long as at least one BTRAP flag is set in register TFR, ATOMIC/EXTEND instructions do not work !

Detailled Explanation:

During ATOMIC or EXTEND sequences, no interrupts, PEC transfers, or class A traps will be acknowledged by the CPU. This is a normal and intended function of these instructions. Class B traps signal illegal conditions during the execution of an instruction. Therefore, class B traps can not be implicitly disabled during ATOMIC or EXTEND sequences, since any class B trap exception condition requires immediate system response: the instruction which caused the exception can not be completed the normal way, and no other instruction of the normal program flow must be executed before the BTRAP exception handling routine has been invoked. In order to enter the BTRAP routine in a defined way, class B traps must be acknowledged by the interrupt system, and the standard DDPs must be in effect. In order to identify a class B trap condition, the B trap flags of register TFR are analyzed by the CPU: as long as any of these flags is set, the function of ATOMIC or EXTEND (bypass standard DPPs) is disabled to allow immediate entry into the BTRAP routine.

This may cause problems in particular within the BTRAP service routine itself. Since all trap flags must be cleared by software, ATOMIC or EXTEND instructions will not work within the BTRAP routine until the corresponding class B trap flag has been cleared.

To avoid problems:

a) always clear the B trap flag at the beginning of the BTRAP routine, or

b) compile/assemble the module which contains the BTRAP routine with the compiler/assembler option where no ATOMIC or EXTEND instructions will be used.